REMARKS

Claims 1-51 are all the claims pending in the application.

Arrangement of the Specification

The Examiner kindly provides guidelines that illustrate the preferred layout for the specification of a utility application. The Examiner notes that these guidelines are merely suggested for the applicant's use.

Nonetheless, the Examiner objects to the disclosure because the layout for the specification does not "follow the guidelines as suggested."

This objection is traversed. The application is presented in a format that is acceptable internationally. There is no requirement in law or rule that requires an amendment to follow suggested guidelines.

Notwithstanding the foregoing, Applicants will invest in such change upon allowance of the claims.

Claim Rejections - 35 USC § 102

Claims 1-3, 5-7, 9-10, 12-19, 21-22, 32-38, 44-51 are rejected under 35 U.S.C. 102(b) as being anticipated by Sirringhaus et al. (WO 01/46987 cited by applicant). This rejection is traversed for at least the following reasons.

The Examiner has cited Applicants' own work, over which the present invention is an improvement. Applicants note that the Examiner has made particular reference to Figure 7 and the disclosure on pages 10 to 25 in Integrated Circuits in his argument that this document discloses the method of claim 1.

Use of a Surface Energy Pattern for ***Two*** Layers

The current text of independent claim 1 references the use of a surface energy pattern to localise the semiconductive material to the third area (as well as to localise the electrically conductive material to the first and second areas). As originally disclosed and as claimed, this feature is intended to distinguish over the technique disclosed in WO01/46987.

In the technique described in the present application, the same surface energy pattern is used to pattern both (1) the conductive layer and (2) the semiconductive layer. First, there is no mention in WO01/46987 of using any surface energy pattern for the semiconductor layer. Second, there is no mention in the reference of a use of the same surface energy pattern that is used for the conductive layer.

In the absence of such teaching, the claim cannot be anticipated.

Claim Rejections - 35 USC § 103

Claims 11, 23-25, 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sirringhaus et al. This rejection is traversed for at least the following reasons.

The Examiner again looks to Figs. 7(a)-7(c) and related text on pages 10-25 for a disclosure of "substantially the claimed method for forming on a substrate an electronic device except the channel length, thickness of substrate, and the process temperature." The Examiner asserts that "those limitations are considered to involve routine optimization."

The Examiner makes no mention of the two missing features as noted above. Such features are neither inherent nor obvious, and would not be attained using routine optimization. They simply are extraordinary and would not be obvious to one skilled in the art.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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